Nokia Customer Care
RM-8/RM-47/RM-48 Series Transceivers

7 - System Module

Table of Contents

Page No

Glossary of Terms

ACIAccessory Control Interface

ADCAnalog Digital Converter

AMSLAfter Market Service Leader

ASICApplication Specific Integrated Circuit

ASIPApplication Specific Integrated Passive

ADSPApplication DSP (expected to run high level tasks)

ARMAdvanced RISC Machines

BB Baseband

CCPCompact Camera Port

CDSPCellular DSP (expected to run low level tasks)

COF Chip on foil

COG Chip On Glass

CSTN Color Super Twisted Nematic

CTSIClock Timing Sleep and Interrupt block of Tiku

DCT4.5 Digital Core Technology, generation 4.5

DSP Digital Signal Processor

EMCElectro Magnetic Compatibility

ESDElectro Static Discharge

FRFull Rate

FSTNFilm compensated Super Twisted Nematic

GSMGlobal System Mobile

HWHardware

IFInterface

IHFIntegrated Hands Free

IMEIInternational Mobile Equipment Identity

IRInfrared

IrDaInfrared Data Association

LCDLiquid Crystal Display

LDOLow Drop Out

LEDLight Emitting Diode

MCUMicroprocessor Control Unit

NTCNegative temperature Coefficient, temperature sensitive resistor used as a temperature sensor.

PAPower Amplifier (RF)

PDAPersonal Digital Assistant

PDRAMProgram/Data RAM (on chip in Tiku)

PhoenixSW tool of DCT4.x

PUPGeneral Purpose IO (**P**IO), **U**SARTS and **P**ulse Width Modulators

PWBPrinted Wired Board

PopPort^{TM}BB4.x system connector. It includes: USB, Stereo headset, Fbus.

RTCReal Time Clock, small circuitry that keeps track of updating the clock counter and the calendar. To keep it update without (or empty) battery, an alternative power source can be used: small battery or large capacitor.

SARAMSingle Access RAM

SIMSubscriber Identification Module

SWSoftware

SWIMSubscriber / Wallet Identification Module

SPRStandard Product Requirements

STISerial Trace Interface

TCXOTemperature controlled Oscillator

TikuSuccessor of the UPP, officially Tiku Edge

UEMEUniversal Energy Management Enhanced

UEMEKSuccessor of UEME

UIUser Interface

USBUniversal Serial Bus

UPPUniversal Phone Processor

Baseband Module Introduction

This chapter describes the baseband module for the RM-8/RM-47/RM-48 program. The baseband module includes the baseband engine chipset, the UI components and acoustical parts of the transceiver.

The RM-8 is a hand-portable EGSM900/GSM1800/GSM1900 phone for the fashion segment. RM-47 (EGSM900/GSM1800/GSM1900) and RM-48 (GSM850/GSM1800/GSM1900) are hand-portable phones for the classic segment. They all have the DCT4.5 generation baseband and RF circuitry. The key driver for these products is the implementation of EDGE, introducing true multimedia capability from WCDMA in GSM single mode.

RM-8/RM-47/RM-48 is equipped with the DCT4 connector, supporting most of the DCT4 accessories. The battery interface is relative new consisting of only 3 connections. Standard battery is BL-4C battery with 760mAh capacity.

Features

The HW specific features of the RM-8/RM-47/RM-48 phone:

- Fold phone with easily exchangeable fabrics.
- Tripleband Engine (900, 1800, 1900) (or 850, 1800, 1900 in RM-48)
- EDGE (EGPRS): MSC 10 (4+2)
- FR, EFR, AMR codecs
- Integrated Camera and Colour Displays
- MMS (Multi Media Messaging), Java MIDP, SyncML & xHTML
- USB Interface to PC
- IrDA
- FM Radio (only in RM-8)
- IHF
- PopPort™ Accessory support

Accessories:

- Chargers: ACP-12, LCH-9, LCH-12 and AC-1.
- Car accessories: HF-3 and BHF-3.
- Audio accessories: HDB-4, HS-5, LPS-4, HS-3, AD-5B and MD-1
- Connectivity accessories: DKU-2 and HDA-10.

Environmental Specifications

Normal and extreme voltages

Following voltages are assumed as normal and extreme voltages for used battery:

Table 1: Normal and extreme voltages

Table 2:

Voltage	Voltage [V]	Condition
General Conditions		
Nominal voltage	3,700	
Lower extreme voltage	3,145	1
Higher extreme voltage (fast charging)	4,230	2
HW Shutdown Voltages		
Vmstr+	2,1 ± 0,1	Off to on
Vmstr-	1,9 ± 0,1	On to off
SW Shutdown Voltages		
Sw shutdown	3,1	In call
Sw shutdown	3,2	In idle
Min Operating Voltage		
Vcoff+	3,1 ± 0,1	Off to on
Vcoff-	2,8 ± 0,1	On to off

[1] ADC settings in the SW might shutdown the phone above this value.
[2] During fast charging of an empty battery, the voltage might exceed this value. Voltages between 4.20 and 4.60 might appear for a short while.

Temperature conditions

- Operational temperature range (all specifications met within this range):
–5°C.. +55°C (stationary use)
- Functional temperature range (reduced performance):
–30°C.. +70°C
- Storage temperature range:
–30°C.. +85°C

Temperatures at –10°C, +25°C and +55°C are used for the cpk analysis.

The baseband module complies with the SPR4 Operating Conditions.

Humidity

Relative humidity range is 5...95%.

The BB module is not protected against water. Condensed or splashed water might cause malfunction. Any submerge of the phone will cause permanent damage. Long-term high humidity, with condensation, will cause permanent damage because of corrosion.

The baseband module complies with the SPR4 Operating Conditions.

Vibration

The baseband module complies with the SPR4 Operating Conditions.

ESD strength

Standard for electrostatic discharge is IEC 61000-4-2 and level 4 requirements are fulfilled.

The baseband module complies with the SPR4 Operating Conditions.

Technical Specifications

UEME

UEME is the Universal Energy Management Enhanced IC for digital hand portable phones. In addition to energy management, the UEME functionality performs all baseband mixed–signal functions.

The different states of the UEME are explained below.

No supply

In the NO_SUPPLY mode the UEME has no supply voltage (VBAT < VMSTR and VBACK<V_BUCOFF-). This mode is due to the fact, that both the main battery and the backup battery are either disconnected or both discharged to a low voltage level.

The UEME will recover from NO_SUPPLY into the RESET mode, if the VBAT voltage level rises above the VMSTR+ level, by either reconnecting the main battery or charging it to such level.

Backup

In the BACK_UP mode the main battery is either disconnected or has a low voltage level (VBAT < VMSTR- and VBACK > V_BUCOFF+).

The regulator VRTC that supplies the real time clock is disabled in the BACK_UP mode. Instead the unregulated backup battery voltage VBACK supplies the output of the VRTC. All other regulators are disabled and the phone has no functionality.

The UEME will recover from the BACK_UP mode into the RESET mode if VBAT rises above VMSTR+.

Power off

In order for the UEME to be in the PWR_OFF mode, it must have supply voltage (VBAT > VMSTR+).

The VRTC regulator is enabled and supplying the RTC within the UEME. The UEME will enter the RESET mode after a 20 ms delay whenever one of the below listed conditions is logically true:

- The power button is activated.
- Charger connection is detected.
- RTC alarm is detected.

The UEME will enter PWR_OFF from all other modes except NO_SUPPLY and BACK_UP if the internal watchdog elapses.

Reset

When the UEME enters the RESET mode from the PWR_OFF mode the watchdog is enabled. If the VBAT fails to rise above the power-up voltage level VCOFF+ (3.1 V), before the watchdog elapses, the UEME will enter the PWR_OFF mode. Otherwise, after a 200 ms delay the regulator VFLASH1 will be enabled and after an additional delay of 500 s, the regulators VANA, VIO, VCORE and VR3 will be enabled. All other regulators i.e. VFLASH2, VSIM, VR1, VR2 and VR4

– VR7 are software controlled and disabled by default. After an additional delay of 20 ms, the UEME enters the PWR_ON mode.

Power on

In PWR_ON the UEME is fully functional in the sense that all internal circuits are powered up or can be by means of software. The UEME will enter the PWR_OFF mode if VBAT drops below VCOOF- for a period of time longer than 5 s. The UEME will furthermore enter the PWR_OFF mode if either of the watchdogs Operational State Machine (approx. 100 s), Security (32 sec.) or Power Key (4 sec.) elapses or if any of the regulators triggers the thermal protection circuitry.

Sleep

The UEME can be forced into the SLEEP mode by the Tiku by setting the input SLEEPX low for more than 60 s. This state is entered when the external Tiku activity is low (phone in sleep) and thereby lowering the internal current consumption of the UEME. The regulator VANA is disabled and VR1 – VR7 are either disabled or in low quiescent mode. From SLEEP the UEME enters PWR_ON if SLEEPX goes high, the PWR_OFF mode if watchdog elapses or the BACK_UP mode if VBAT drops below VMSTR-.

Protection mode

The UEME has two separate protection limits for over temperature conditions, one for the charging switch and one for the regulators. The temperature circuitry measures the onchip temperature. In case of charging over temperature, the circuit turns the charging switch off. In case of over temperature in any of the regulators, the UEME powers off.

DC Characteristics

The figures in the following table reflect the specification of the voltage and current regulators within the UEME.

Table 3: UEME Regulator Output and State in Sleep

Table 4:

Name	Voltage (V)			Current (mA)		Filter	Comment
	Min	Nom	Max	Max	Sleep Max		
VANA	2.70	2.78	2.86	80		2	5uA minimum for stability. Controlled by the UEME. Disabled in Sleep mode.
VFLASH1	2.61	2.78	2.95	70	1.5	1	5uA minimum for stability. Controlled by the UEME.
VIO	1.72	1.80	1.88	150	0.5	3	5uA minimum for stability. Controlled by the UEME.
VCORE	1.41	1.50	1.59	200	0.2	1	5uA minimum for stability. MCUSW is setting the voltage.
VAUX1	1.745 2.91	1.80 3.0	1.855 3.09	50	0.5	1	Voltage level is set by MCUSW.
VAUX2	2.70	2.78	2.86	70	0.5	1	5uA minimum for stability.
VAUX3	2.70	2.78	2.86	10	0.5	1	5uA minimum for stability.
VSIM	1.745 2.91	1.80 3.00	1.855 3.09	25	0.5	-	5uA minimum for stability.
VR1A/B	4.60	4.75	4.90	10	-	4	Disabled in Sleep mode. The maximum current is for 1 regulator active. If both are used, maximum 5mA each.
VR2	2.70 (2.61)	2.78 (2.78)	2.86 (2.95)	100	-	5	100uA minimum for stability. Active during (Sleep-mode).
VR3	2.70	2.78	2.86	20	-	4	100uA minimum for stability. Controlled by the UEME.
VR4	2.70	2.78	2.86	50	0.1	6	100uA minimum for stability.

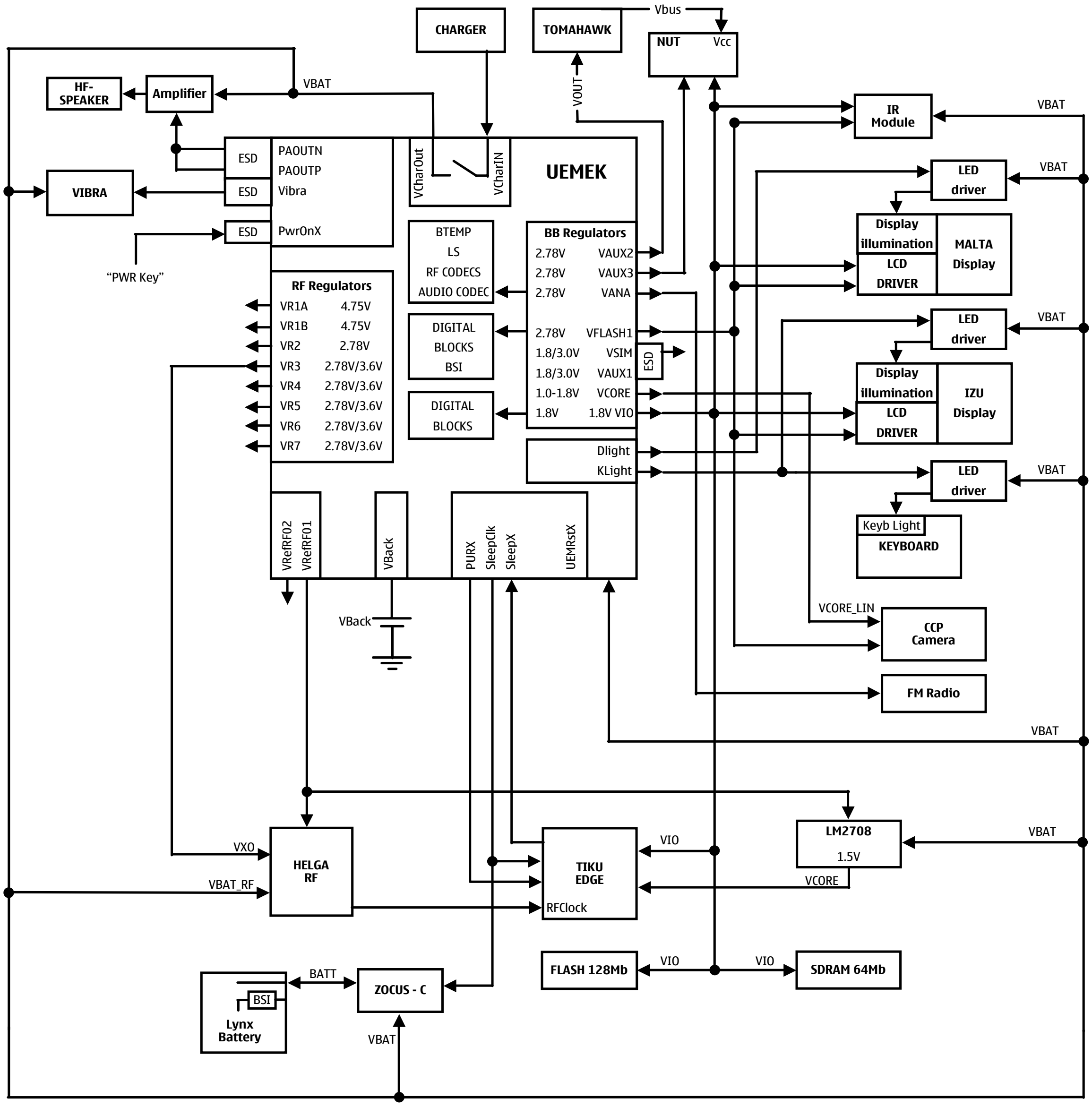
Table 4:

VR5	2.70	2.78	2.86	50	0.1	7	100uA minimum for stability.
VR6	2.70	2.78	2.86	50	0.1	7	100uA minimum for stability.
VR7	2.70	2.78	2.86	45	-	7	100uA minimum for stability.

Power Distribution

The connection of the miscellaneous power connection can be seen in the following overview.

Figure 1:Power distribution



Tiku

This is the main digital baseband ASIC.

Main Features

The Tiku consists of the following sections:

- Arm 925 MPU
- A-DSP (Lead3 for Application sw – 4KB ApiRam, 128KB saram, 32KB daram)
- C-DSP (Lead3 for Cellular sw – 4KB ApiRam, 128KB saram, 32KB daram)
- DSP Co-processors (DCT and Motion Estimator) on both DSP
- Corona EDGE hardware accelerator
- Serial flash interface (SFI001)
- 2G Body logic, as in UPP-WD2
- 4Mb of pdram.
- Traffic controller for memory interface (dct4 flash/sram, sdram)
- General purpose USARTs
- SIM card interface
- 2nd SIM interface (used for MMC)
- I^{2}C interface (used for FCI)
- GSM coder
- Interface control for: keyboard, LCD, Camera, audio and UEME control
- Accessory interfaces: IrDa and LPRF (Bluetooth)
- Handling of RF-BB interface
- I/O voltage = 1.8V, Core voltage = 1.5V
- 288 pins uBGA, 0.5mm pitch, 12 mm x 12 mm package

The Brain consists of 5 sections; the ARM925 Mega-Module, (consisting of the ARM9 MCU, Cache memory, Parallel LCD Controller, and Traffic Controller), C-DSP Lead 3 Mega-Module, A-DSP Lead 3 Mega-Module, PDRAM, and PDA Peripherals.

The ARM-Mega-Module has a Traffic controller, which provides the interface between the MCU, external memories, LCD controller, and internal busses. It also processes the data packages for memory access.

The PDA Peripherals consists of Camera Compact Port (CCP) interface, Multi-Media Card (MMC), IR, USB, and Display interfaces.

Memory Block

For the MCU, TIKU includes ROM, 2 kbytes, that is used mainly for boot code of MCU. For the program memory, 4Mbit (256K x 16bit, organized as 8 banks of 64Kb) PDRAM is integrated. RAM is mainly for MCU purposes. The MCU can also store a code into the external flash memory, which consist of one NOR flash and one NAND flash. The size of the NOR flash is 128Mbit (8Mbit x16bit) and it's used for primary application code. The secondary flash is a NAND flash, which is used for slow accessible data such as user-settings, pictures, ringtones etc. (non speed dependent code). The size of the NAND flash is 64Mbit (4096K x 16 bit).

Memory

The external memory interface consists of two types of memory, used for different purposes.

NOR Flash

The NOR flash is used as the primary data storage. Here the MCU SW package is stored.

Furthermore, the memory is capable of handling burst mode (multiplexed address/data-bus) and memory blocking, which is controlled by TIKU.

RM-8 has a flash memory size of 128Mbit + 128Mbit = 32MB. There are two NOR flash chips in the same package. They have individual chip selects. The second chip is for user data only.

RM-47 has a flash memory size of 128Mbit = 16MB. The second flash chip is not fitted in the memory package. Both MCU SW and user data are in the same memory chip.

SDRAM

The SDRAM is used as a data handling memory.

The SDRAM interface to TIKU is different than the 24 lines multiplexed data/address bus used for the flash memory. First the address is set up then the data is latched out in a normal asynchronous/synchronous way. In the synchronous mode, the data is clocked out at a maximum frequency at 123MHz.

Charging

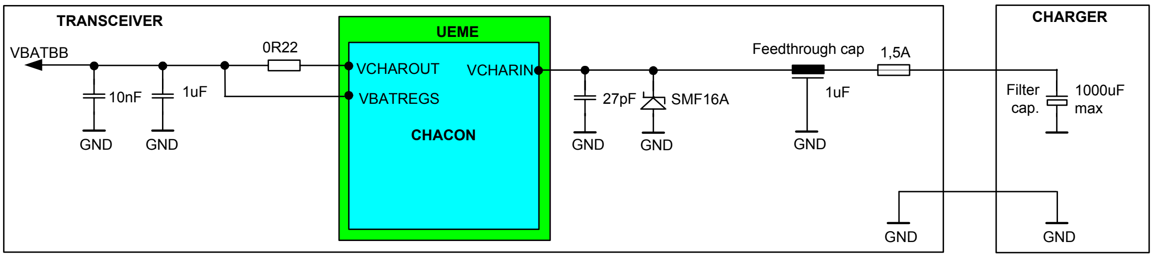
The RM-8/RM-47/RM-48 program conforms to the global NMP Charger Interface.

This comprehensive interface ensures future proofing should new chargers become available.

Charging is controlled by the UEME and external components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The DCT4.5 baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. 3-wire chargers are treated as 2-wire (PopPort^{TM} specifications).

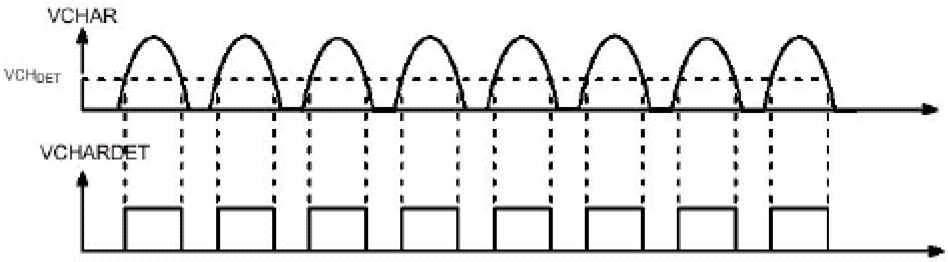
The operation of the charging circuit has been specified in such a way as to limit the power dissipation across the charge switch and to ensure safe operation in all modes.

Figure 2:Charging



Connecting a charger creates voltage on VCHAR input. When VCHAR input's voltage level is detected to rise above the VCHDET+ threshold by CHACON, the charging starts. The VCHARDET signal is generated to indicate the presence of the charger. However, detection output signal must be gated always to a logical '0' when MSTRX='0', in order not to force logical high level to the UEME's internal blocks that are not supplied at the time. Level crossing detection of the VCHAR line is used to generate synchronizing pulses for UEME's state machine for control of rectifier type chargers. The VCHARDET output gives a logical '1' when the VCHAR input is detected to be above the VCHDET+ level and '0' when the VCHAR input level is below VCHDET.

Figure 3:Detection of charger / generation of charger synchronisation pulses



In case the main battery is fully discharged and the UEME subsequently is without power, i.e. in NO_SUPPLY or BACKUP mode, the start-up charging circuitry is in control, giving the possibility to detect a charger and engage charging. If the VBAT level is detected to be lower than the master reset voltage (VMSTR-) the CHACON will charge the battery with a constant current of 100 mA until VBAT exceeds VMSTR+. When this happens, from a charging point of view, normal PWM charging situation resumes. A PWM signal is generated by the digital part of the UEME, which sources the CHACON. The frequency of the signal can be either 1 Hz or 32 Hz. If the connected charger is of a 2-wire kind, e.g. ACP- 7, the PWM signal has the frequency of 1 Hz. If the charger on the other hand is a 3-wire type, e.g. LCH-9, the switch is left on permanently and the 32 Hz PWM control signal is routed to the charger in order to produce a constant voltage.

Battery

Type: BL-4C

Technology: Li-Ion. 4.2V charging. 3.1V cut-off

Capacity: 760 (BSI=75K)

The battery is a Li Ion based standard cell with LiMnO chemistry.

This type of battery has a three-pin connector (BTEMP is not used).

Figure 4:BL-4C Battery

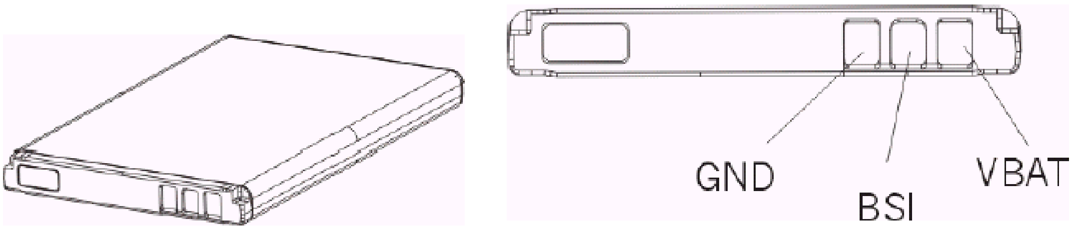


Table 5: BSI Levels BL-4C Battery

Table 6:

Mode	BSI (kOhm /			Description
	Min	Type	Max	
Normal		75		Used for calculating the Capacity (BL-4C 760 mAh)
Service	3.2	3.3	3.4	Pull-down resistor in battery. Used for fast power-up in production (LOCAL mode), R/D purposes or in aftersales, 1% tolerance resistors shall be used.
Test	6.7	6.8	6.9	Pull-down resistor in battery, used in production for testing purposes. 1% tolerance resistors shall be used.
Banned			<3.2	

Inside the battery, an over-temperature and an over-voltage protection circuit are implemented.

Care should be taken with the temperature. If the battery is charged above 60 degrees Celsius, overheating might occur.

Interfaces

FM-Radio

FM radio is in RM-8, but has not been assembled in RM-47 or RM-48.

The FM radio circuitry is implemented using a highly integrated radio TEA5761. The MCU SW controls the FM radio circuitry through serial bus interface.

The stereo output is fed to the UEME MIC3 on the microphone input.

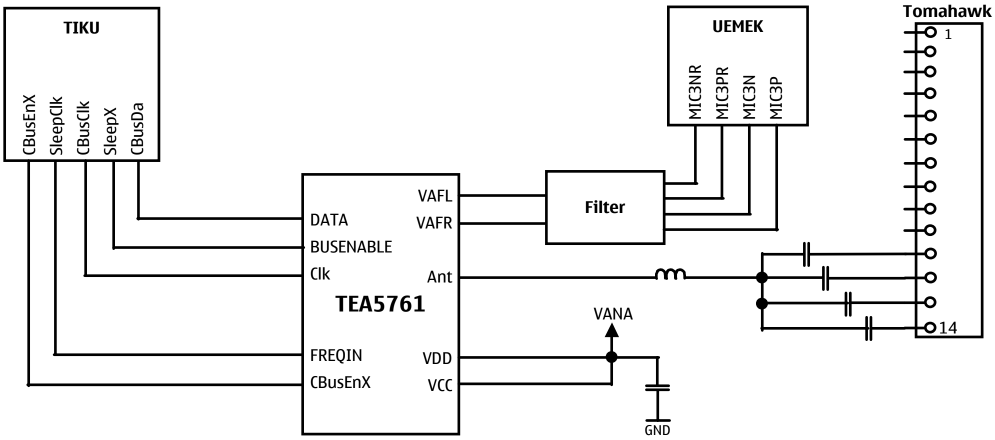
The antenna of the FM Radio is created with the headset. The wires of the headset are used as poles of the antenna.

While W/R (WRITE/READ) is HIGH the TIKU can transmit data to the TEA5761. At the rising edge of the Bus clock, the register shifts and accepts the stable bit. At clock low the TIKU writes the following bit. A tuning function is started when the W/R signal changes from HIGH to LOW. Was a search tuning requested sent, the IC autonomously starts searching the FM band. Search direction and search stop level can be chosen. Was a station with a fieldstrength equal or higher than this stop level found, the tuning system stops and the Found Flag bit is set to “HIGH”. Was during search a band limit reached, the tuning system stops at the band limit and the Band Limit flag bit is set to high. Also the Found Flag is set to high in this case.

While Write/Read is “LOW” the Tiku EDGE can read data. At the rising edge of the BUS Clock, data will be shifted out of the register. This data is available from the point where the bus clock is HIGH until the next rising edge of the clock occurs.

Interface to Engine

Figure 5:FM radio block diagram



IrDA

The RM-8/RM-47/RM-48 phone supports data connectivity via the Infra Red link. The IR interface is integrated into the TIKU and the main external component is the IR module. The datarate supported will be 1.152Mbit.

Interface to Engine

This interface receives data from and transmits data to peripheral equipment. It transforms serial data to parallel data for the MCU or DSP and vice versa. The IAccIF IR interface is divided into two blocks, MIR and FIR. IR is a UART-based block for baud rates in the range 9600 bit/s to 115.2 kbit/s, and FIR is for the 1.152 Mbit/s rate. Both parts have the same physical connections so they cannot be used simultaneously. The shut down pin SD can power off the module.

The maximum distance in the RM-8/RM-47 phone configuration is approximately 20 centimetres.

The SIR block (9600 bit/s to 115.2 kbit/s):

- Supports IrDA format with speeds up to 115.2 kbit/s

- Supports Phonet format, having all the same baud rates (9600 bit/s – 115.2kbit/s) as Fbus.

The FIR block (1.152 Mbit/s):

- Supports IrDA format with baud rate 1.152 Mbit/s.
- Both these blocks are sub-divided into IR transmitter and IR receiver. Interconnection details are shown in the following figure and table.

Figure 6:IRDA Interconnections between Tiku and UEME

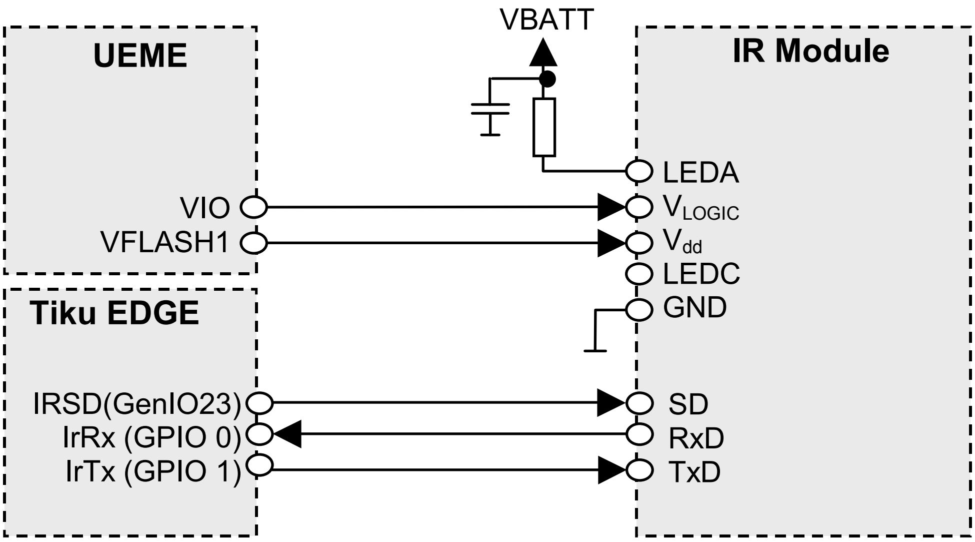


Table 7: IRDA connections between Tiku EDGE and the IR module

Table 8:

Name	I/O	Engine connection		Description
TXD	O	TIKU	GPIO1: [IRTx]	Transmitted data output to IR Module
RXD	I	TIKU	GPIO0: [IRRx]	Received data input from IR Module.
SD	O	TIKU	GenIO23: [IRSD]	IR Module shut down.
VLOGIC	O	UEME	VIO	Supply voltage for digital parts, 1.8 V.
VCC	O	UEME	VFLASH1	IR Module supply voltage, 2.78 V.
LEDA	O	VBATT		IR LED Anode supply voltage.

Camera

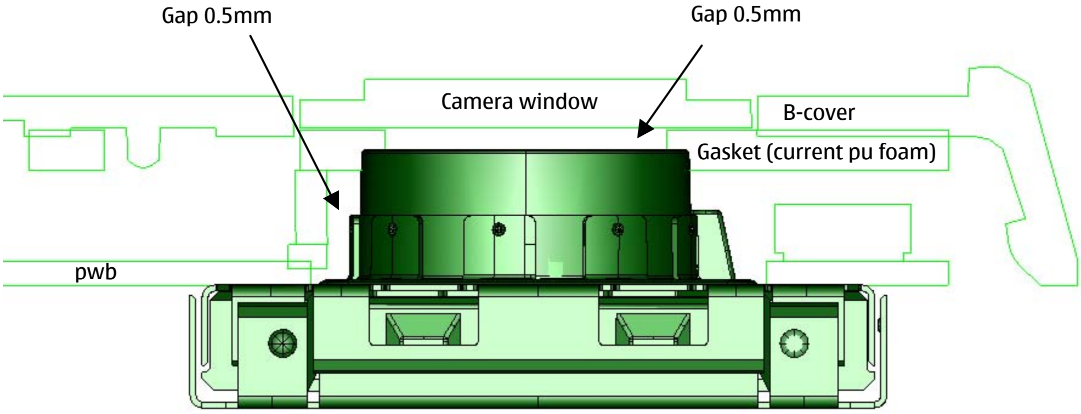
The RM-8/RM-47/RM-48 phone is equipped with a VGA resolution camera with an active area of 660H x 492V. Pictures delivered to engine are standard VGA (640 x 480). This camera is able to transfer up to 30 frames per second in the viewfinder mode and 15 frames per second in full resolution mode (VGA). Full resolution pictures are in RGB 5:6:5 or YUV 4:2:2 (10 bits raw sensor resolution). The camera used is a VV6652 module.

Mounting

The camera is placed physically almost inside the antenna on the backside of the phone upper block PWB. The camera fixture (spring type, see the figure below) is located between the RF shielding cans. Shielding is done in a combination of metalized plastic housing of the camera module and ground connected spring/clip fixture.

Experience shows that good shielding is necessary. The metalized housing and the spring/clip will shield the camera. The hole for the lens is kept as small as possible to avoid direct EMC entrance into camera module by lens opening.

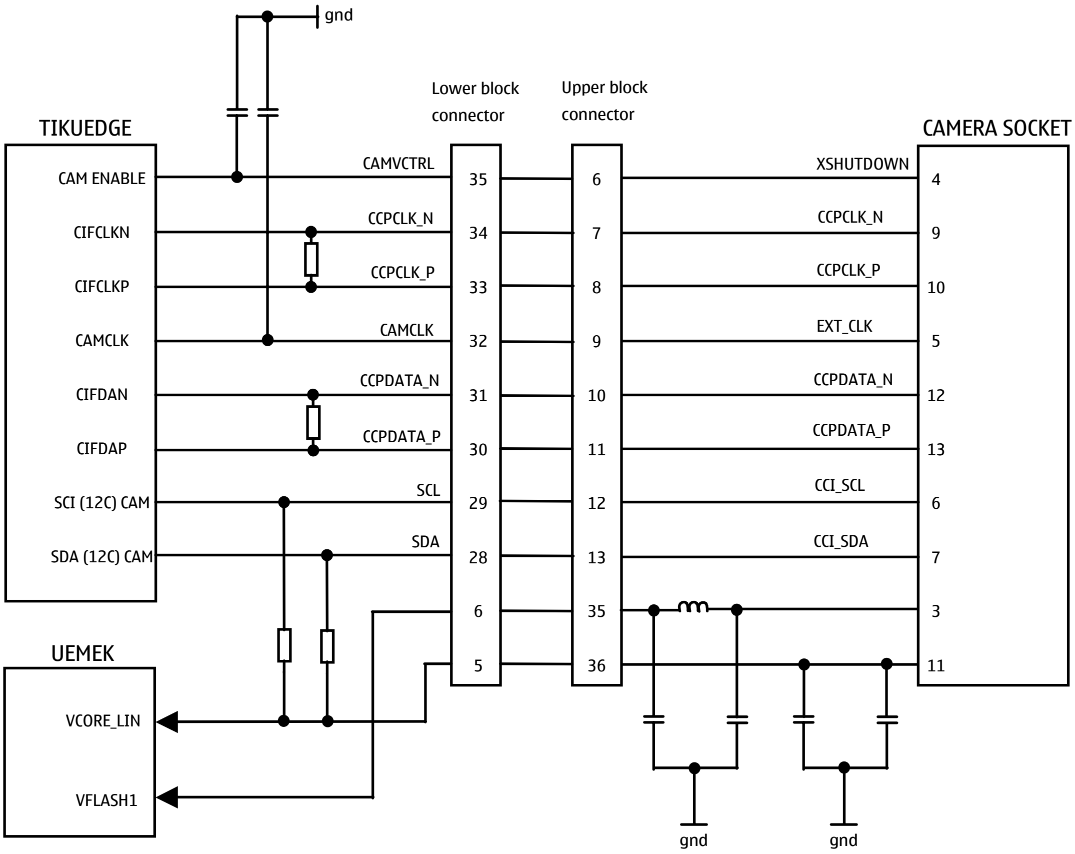
Figure 7:Camera Module Mounting



Interface to Engine

The camera is connected to the TIKU via a dedicated differential camera bus called CCP. The control of the camera is routed through normal-type general I/O ports. The camera uses 2 different supplies; analog and digital supply.

Figure 8:Camera Interface



Power supply to the camera module doesn't need to be shut down when the camera is in the standby mode. The camera uses very low stand-by current.

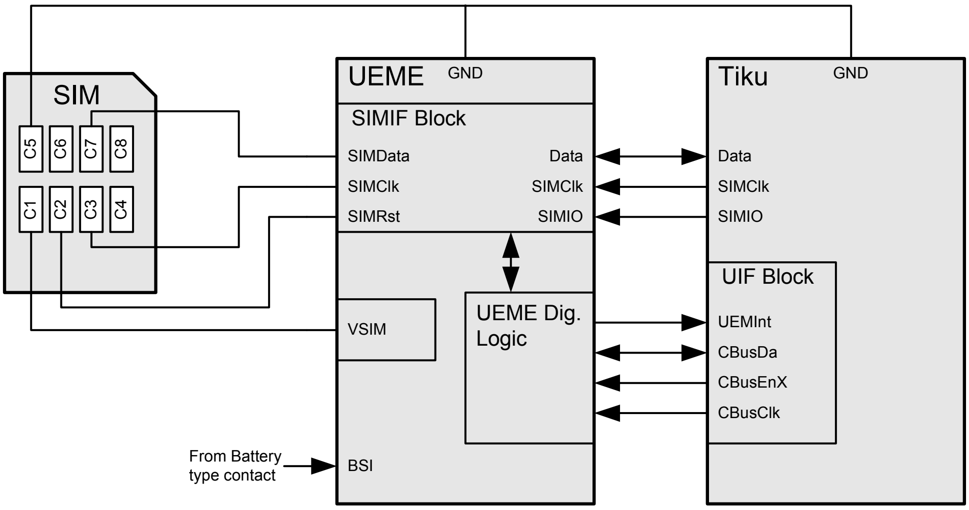
SIM

The UEME contains the SIM interface logic level shifting. The SIM interface can be programmed to support 3V and 1.8V SIMs.

The SIM interface is powered up when the SIMCardDet signal indicates, ”card in”. This signal is derived from the BSI signal.

Interface to Engine

Figure 9:TIKU/UEME SIM Interface Connections



The internal clock frequency from the CTSI Block is 13 MHz in GSM.

Figure 10:SIM Interface Data

Characteristics	Condition	Min	Typ	Max	Unit
SIMPwr, Vcc	on	1.6	1.8	2.0	V
		2.8	3.0	3.2	V
MoneyPwr (5 V), Icc	5 MHz	10			mA
SimPwr(3 V),Icc	4 MHz	6			mA
MoneyPwr(5V), Spikes on Icc (max duration 400 ns)	on			100	mA
SimPwr(3V), Spikes on Icc (max duration 400 ns)	on			50	mA
SimData, MoneyData, SimClk,MoneyClk,SimRst,MoneyRst, V_{OH}		0.9 x Vcc		Vcc	V
SimData, MoneyData,V_{IH}	(External pull–up resistor 20k to Vcc)	0.7 x Vcc		Vcc	V
SimData, MoneyData,V_{IL}		0		0.15 x Vcc	V
SimData, MoneyData,V_{OL}	I_{IL} = 1 mA ***	0		0.15 x Vcc	V
SimData, MoneyData,I_{IH}	V_{IH}	20			μΩ
SimData, MoneyData,I_{OH}	V_{OH}	20			μΩ
SimData, MoneyData,I_{OL}	V_{OL}	20			μΩ
SimData,MoneyData, t_R/t_F	C_{IN} = 30 pF; C_{OUT} = 30 pF			1	μs
SimRst,MoneyRst	C_{OUT} = 30 pF			1	μs
SIMCLK frequency		1.05		3.36	MHz
SimClk,MoneyClk,t_R/t_F	C_{OUT}= 30 pF			26	ns
SimClk, MoneyClk,I_{OH}	V_{OH}	100			μΩ
SimClk, MoneyClk,I_{OL}	V_{OL}	20			μΩ
SimRst, MoneyRst,I_{OL}	V_{OL}	20			μΩ
SimRst, MoneyRst,I_{OH}	V_{OH}	150			μΩ
The voltage on Clock, Data and Rst shall remain between –0.3V and Vcc + 0.3 V .					

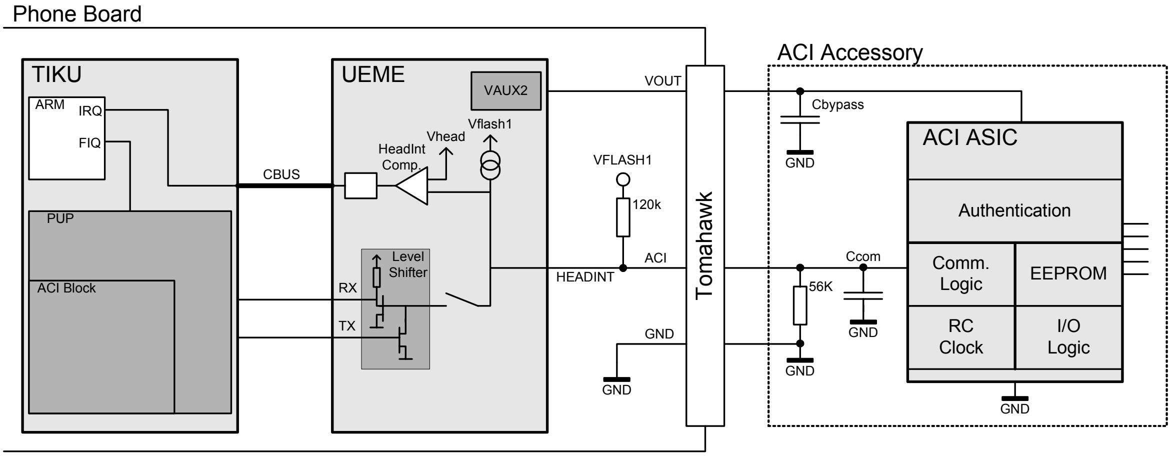
Accessorey Interface (ACI)

ACI (Accessory Control Interface) is a point-to-point, Master-Slave, bi-directional serial bus. ACI supports the following features:

- The identification of accessory type is provided
- The insertion and removal detection of an accessory device
- Providing power to the accessory: 200mW Power out
- Reference voltage to the accessory

The insertion / removal detection is provided by the HeadInt input.

Figure 11:ACI schematics



The Vout pin on the PopPort^{TM} provides external power to accessories. The Vout is supplied by VAUX2 and can be controlled by the UEME. VAUX2 is short circuit protected.

Table 9: Vout specifications

Table 10:

Name	Voltage (V)			Current (mA)		Filter	Comment
	Min	Nom	Max	Max	Sleep Max		
VAUX2	2.70	2.78	2.86	70	0.5	1	

FBUS

More intelligent accessories can use the serial FBUS connection.

These devices can use Vout as the power supply and ACI for identification.

FBUS is an asynchronous data bus having separate TX and RX signals. Default bit rate of the bus is 115.2 Kbit/s. FBUS is mainly used for controlling the phone in the production and for interface to PC via serial cables. Tiku can also support fast bus. This is FBUS with a bitrate of 1.2Mbit.

Fbus is using the same pins as the USB connection.

Table 11: Fbus signals

Table 12:

Name	Name	Voltage (V)			Comment
		Min	Nom	Max	
FBUS RX	VIH	1.95	2.78	3.00	0.7*VFLASH1
	VIL	0	0.20	0.83	0.3*VFLASH1
FBUS TX	VOH	1.95	2.78	3.00	0.7*VFLASH1
	VOL	0	0.20	0.83	0.3*VFLASH1
Rise Time				12.5ns	For Rx and Tx signals

USB

The Nokia USB device solution is supported using the Wireless 2 Function Controller (W2FC) core. This core is included in the TIKU ASIC. The core completes several USB functions automatically and is controlled by the ARM9 MCU.

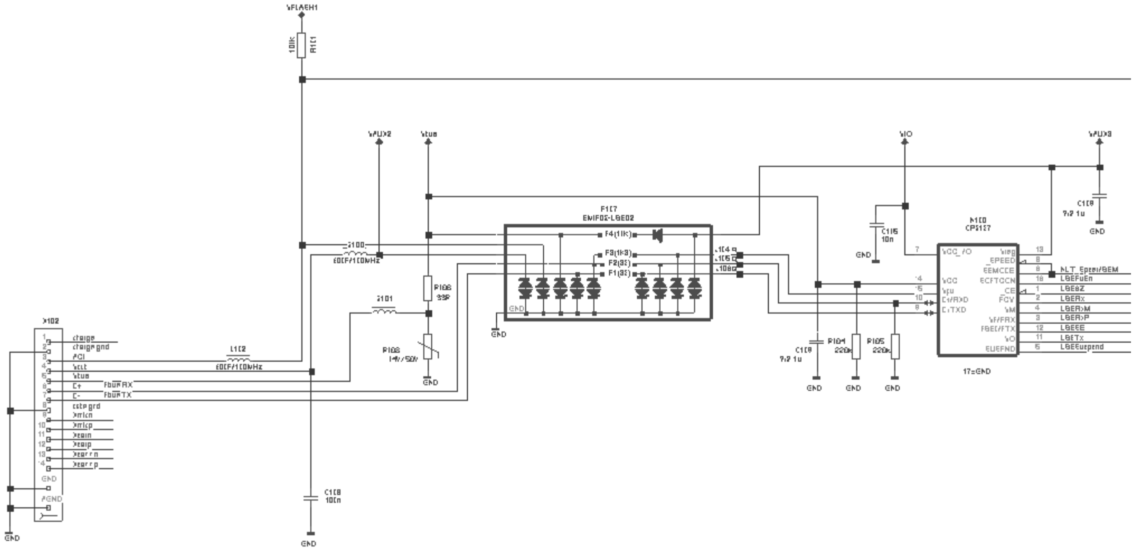
NUT provides the interface between the ASIC's 1.8 V bus and the 3.3 V USB bus. In addition, NUT is capable of transmitting and receiving Fbus signals to and from the Fbus UART in Tiku.

Nokia USB Transceiver (NUT) is fully compliant with the Universal Serial Bus Specification Rev. 1.1.

NUT is able to transmit and receive serial data at full-speed (12 Mbit/s).

The USB signal ESD protection and line matching resistance, and USB pull-up resistor is included to the USB ASIP. This component also includes ESD protection for VOUT and ACI system connector pins.

Figure 12:USB Circuit



UI Interface

Keyboard and Navigator

The RM-8/RM-47/RM-48 phone consists of a mainboard (lower block PWB 1DN) with interface to the upper block PWB 1DS. The connection between the main board and the upper block board is via a hinge flex.

The RM-8/RM-47/RM-48 phone doesn't have a separate keyboard PWB. The keys are connected directly to TikuEdge inside lower block PWB 1DN.

Figure 13:Keyboard layout with special keys for Navi_Up, Navi_Down and Navi_Select

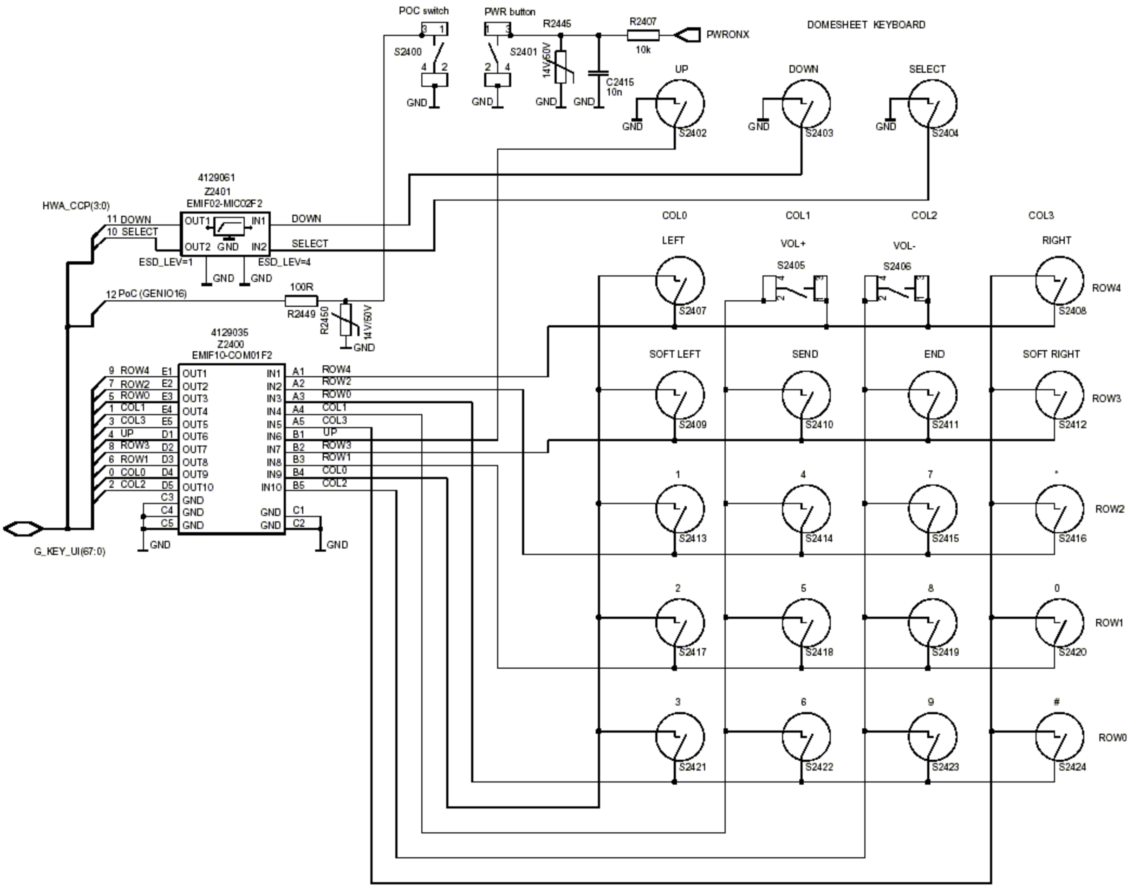


Table 13: Keyboard allocation Tiku GPIO

Table 14:

Keypad matrix and Navigation key		Tiku connection		Description
Navigation Key	Left	Tiku	-	Separate controllines (Special keys) for Navi_Up, Navi_Down and Navi_Select. Navi_Left and Navi_Right are connected to the keyboard matrix
	Up		GPIO 6	
	Right		-	
	Down		GPIO 7	
	Select		GPIO 13	
	GND		-	
Keypad	Column 0	Tiku	GPIO 2	Tiku, Keyboard interface KDI in the UIF block,
	Column 1		GPIO 3	
	Column 2		GPIO 4	
	Column 3		GPIO 5	
	Row 0		GPIO 8	
	Row 1		GPIO 9	
	Row 2		GPIO 10	
	Row 3		GPIO 11	
	Row 4		GPIO 12	

Display Unit

Hardware Interface:

The main display unit interface is a parallel interface consisting of the following:

- 8-bit data bus (DISPDATA(7:0))
- Write enable WRX
- Read enable RDX

Internally, the TIKU DIF block has interfaces with the VIA bus and the secondary DMA controller.

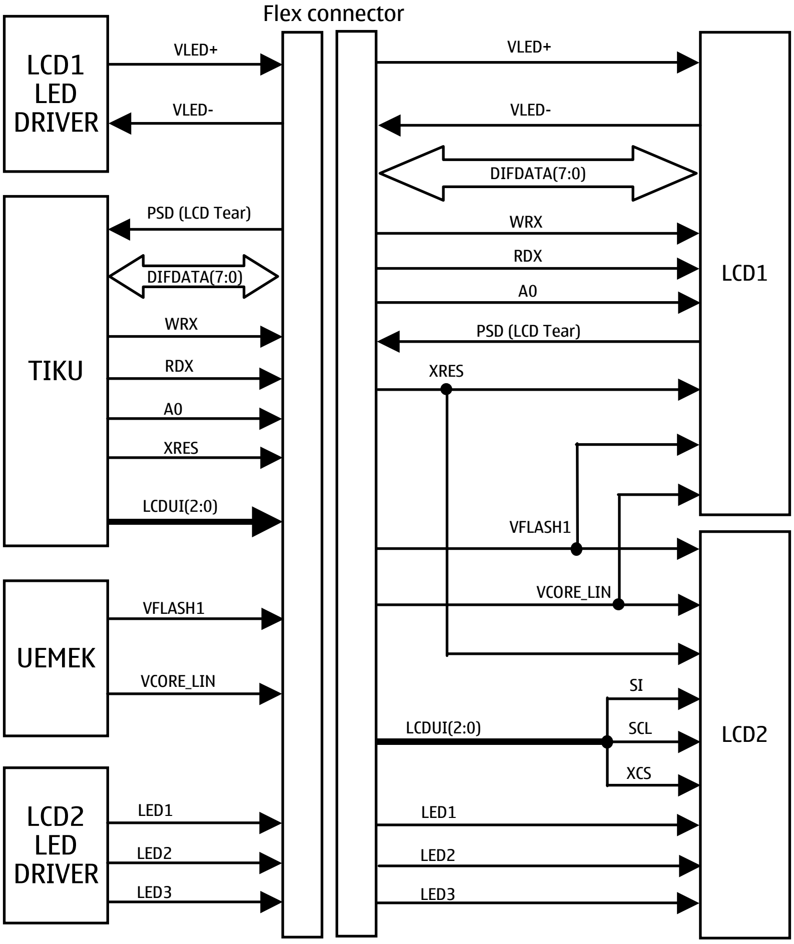
Secondary display (Malta 2) uses a 3-wire serial interface.

Chip-select XCS (active low) enables and disables the serial interface. RESX (active low) is an external reset signal. SCL is serial data clock. SI data-length is 8 bits + D/C-bit.

First bit is a D/C-bit, which indicates the status of the following 8 data bits. In case of a command, D/C-bit is low ('0'). VDDI is supply voltage for the display logic and I/Os. VDD is the supply voltage, from which the display driver generates higher voltages needed to turn the liquid crystals.

Interconnection details are shown in the figure below.

Figure 14:Display Unit Connections



Multiple-keypress:

The RM-8/RM-47 phone will implement multiple keypress. By multiple keypress means the ability to detect that the user has pressed several keys simultaneously. The incitement for implementing this functionality is mainly the support for Java and the requirements set by games.

UI software is capable of supporting multiple keypress, while core SW will have to incorporate this feature into the keyboard driver.

With the current implementation, the design supports 2 simultaneously arbitrarily pressed keys in the keyboard matrix, together with any combination of Navi_Up, Navi_Select and Navi_Down (The special keys).

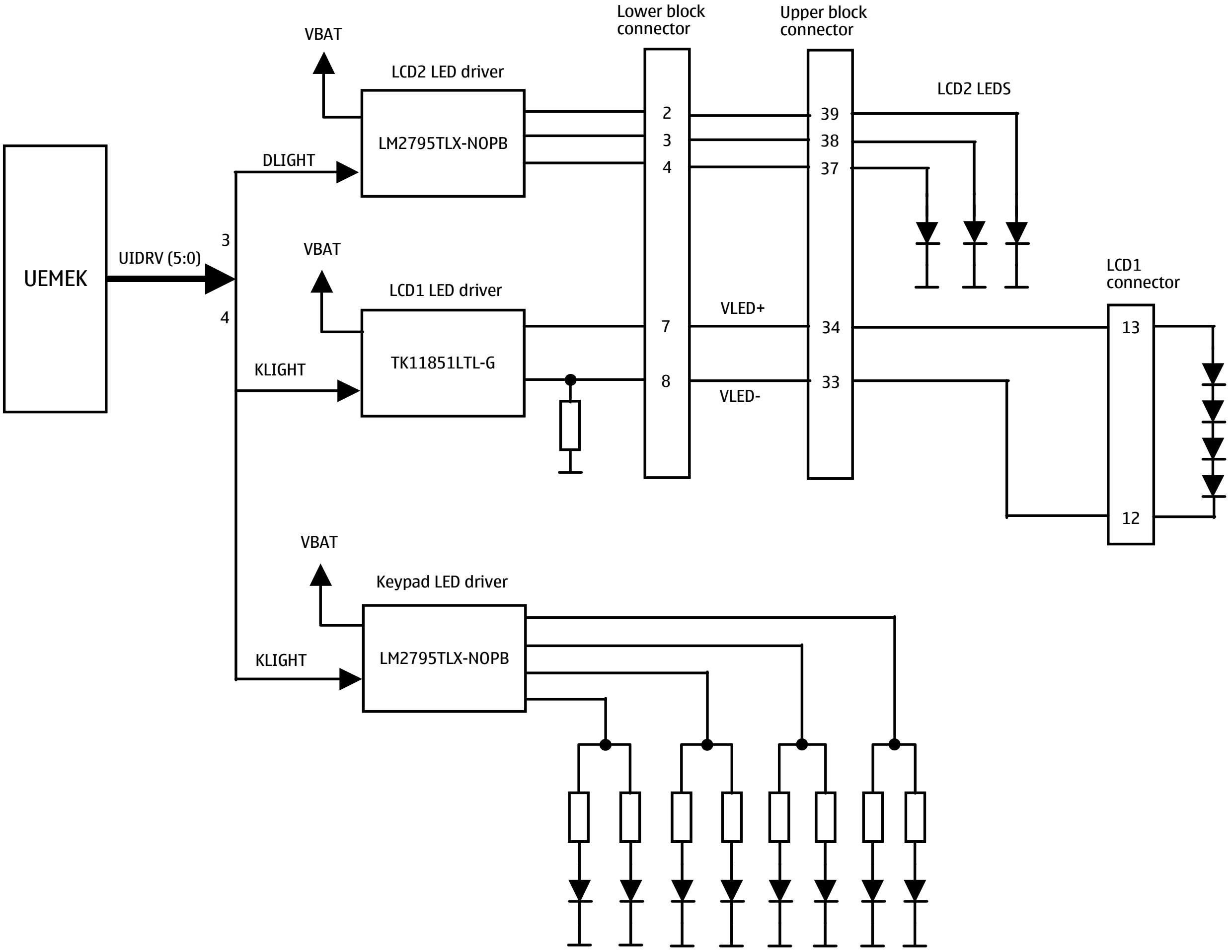
LED Driver

The RM-8/RM-47 phone UI has two sets of LED's soldered on PWBs:

- 3 pcs. for secondary LCD – LED: White
- 8 pcs. for Keyboard – LED: White in RM-8, blue in RM-47 and RM-48

Both groups are individual controllable by the PWM output signal from UEME ASIC.

Figure 15:.LED driver block



Intensity Control:

LEDs are controlled by the PWM output from UEME UI block. The PWM controls can be adjusted in 8-bit step (256). The TK11851L contains a sleep mode. This mode is achieved when the Dlight signal is low.

Vibra

A vibra-alerting device is used to generate a vibration signal for an incoming call. The vibra is placed in the top of the phone. It is placed in the D-cover next to the microphone.

The vibra is electrically connected to the PWB by spring contacts.

The vibra is controlled from the UEME by a PWM (Pulse Width Modulated) square wave signal.

IHF-speaker

Alerting tones and/or melodies are generated by an Internal HandsFree speaker, which is controlled by a PWM signal from the UEME.

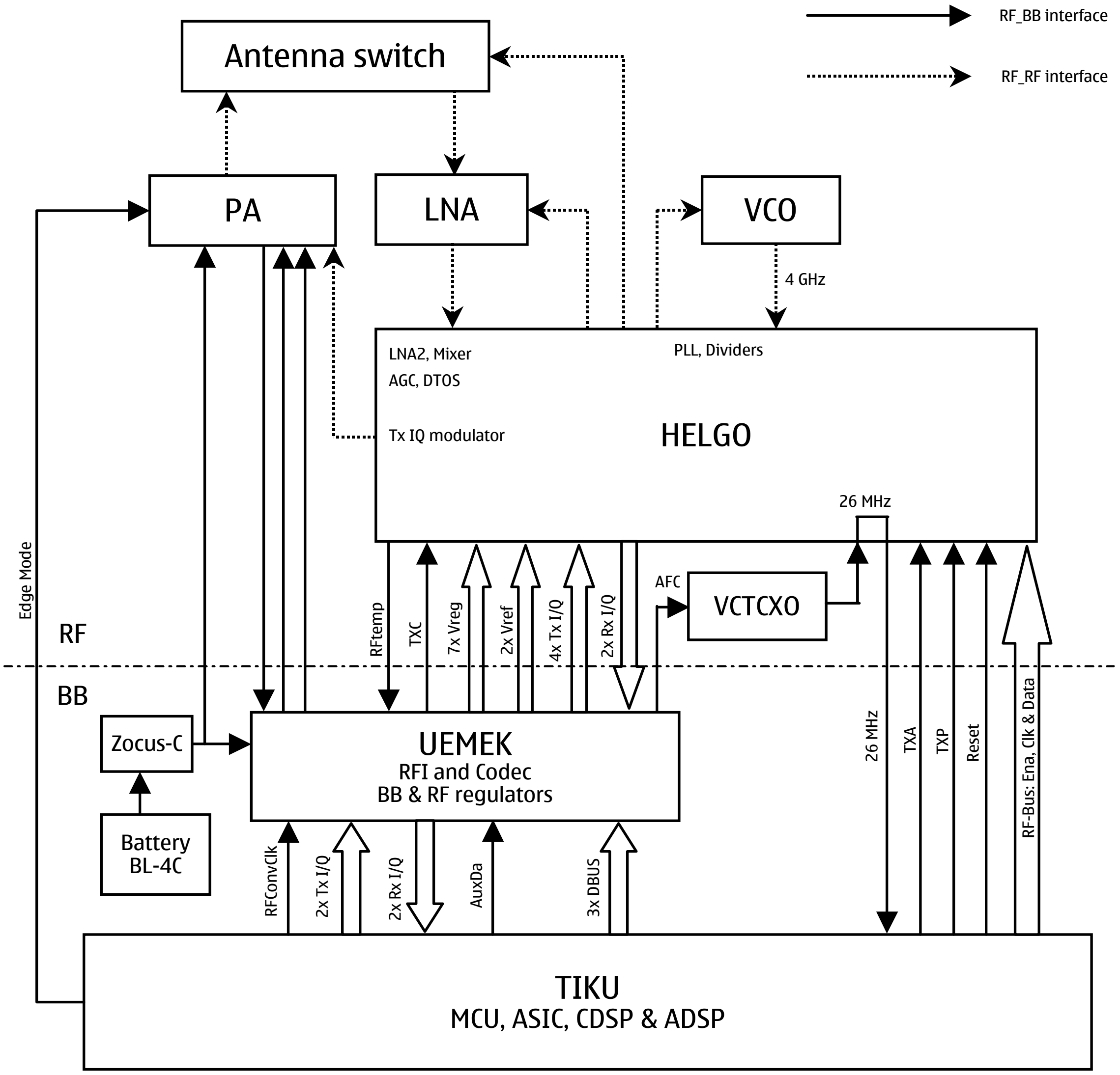
The differential signal from UEME to IHF speaker is amplified by 8 dB with an external amplifier.

The ringer melodies will be optimised in MCU so the main frequency of any given melody is shifted to near the resonant peak. The sound hole is placed in the upper block B-cover. The IHF is electrically connected to the PWB by spring contacts.

RF Interface

The interface between baseband and the RF section is shown below:

Figure 16:Simplified RF/BB Interface Block Diagram



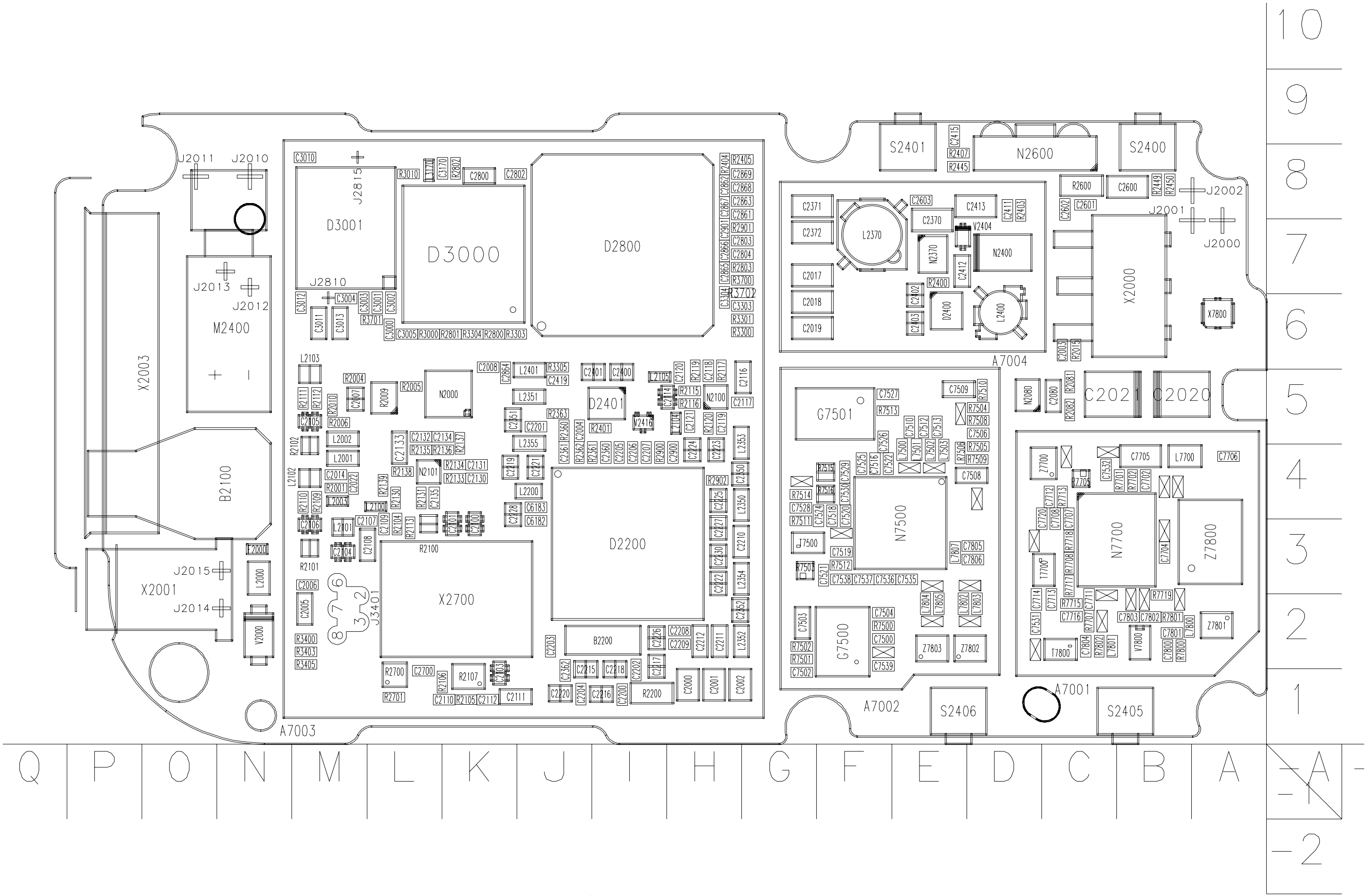
Test Pattern

Test pads are placed on engine PWB for service.

RM-8/RM-47 has adopted the two-row test pattern layout. The basic test pads (FBUS_TX, FBUS_RX, VPP, MBUS & GND) are included.

For specific test pad placement, please see the figure below.

Figure 17:Production Test Pattern

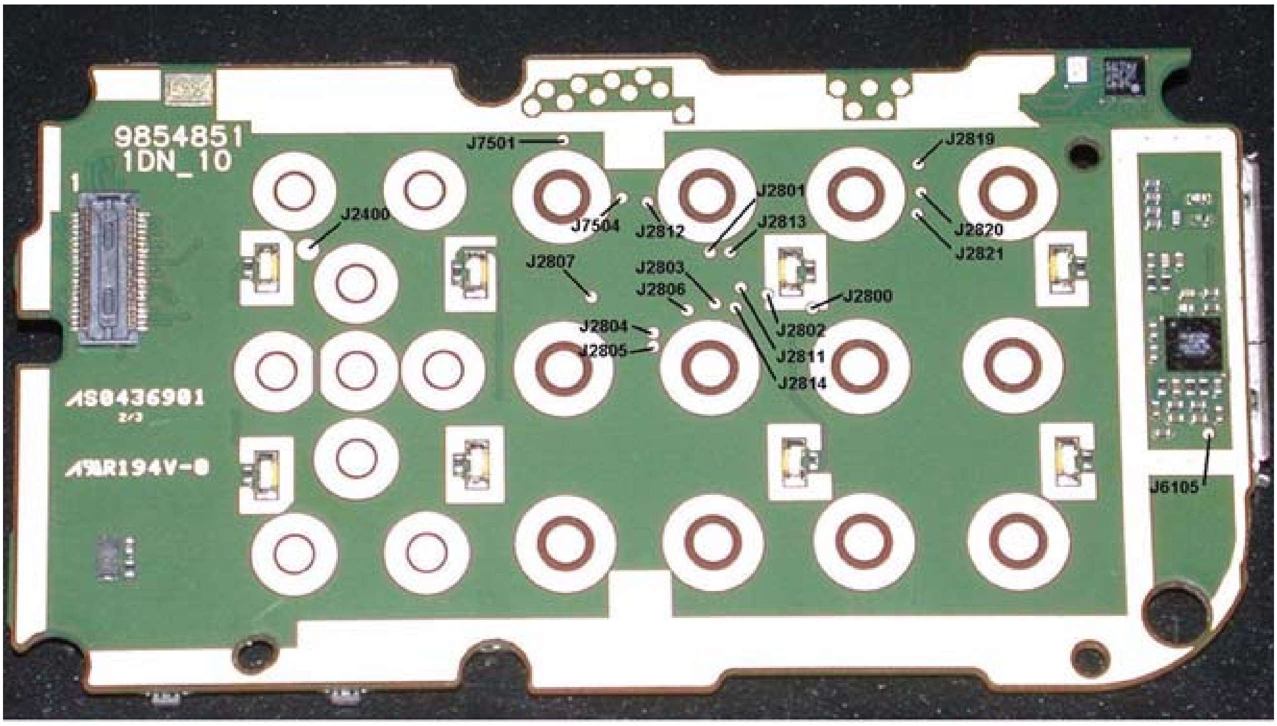


2: TXD/FBUSTXO
3: RXD/FBUSRXO
6: VPP
7: SCK/MBUS
8: GND

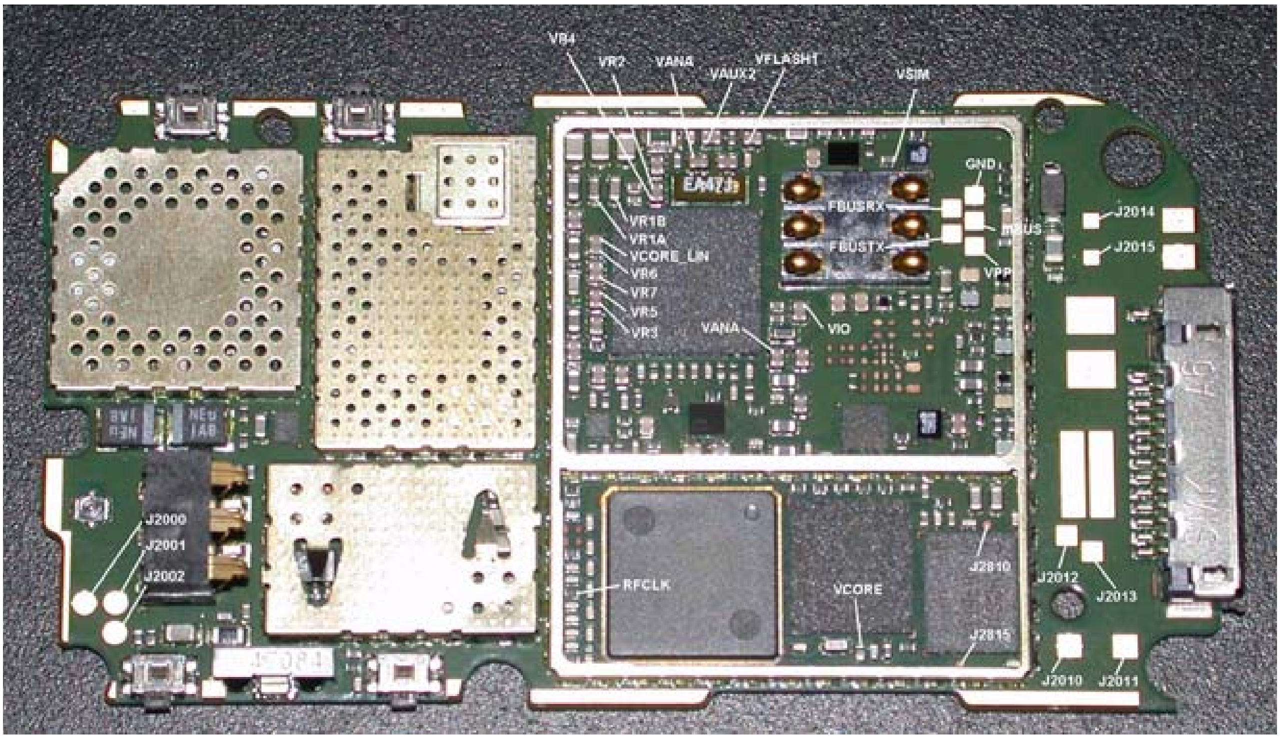
Test Points

See the following two figures for an indication as to where some of the test points can be found.

Main board A side of PWB



Main board B side of PWB



RF Module Introduction

The RF module performs the necessary high frequency operations of the EGSM900/GSM1800/GSM1900 triple band (EDGE) engine in the RM-8/RM-47 product and GSM850/GSM1800/GSM1900 in RM-48.

Both, the transmitter and receiver have been implemented by using direct conversion architecture, which means that the modulator and demodulator operate at the channel frequency.

The core of the RF is an application-specific integrated circuit, Helgo. Another core component is a power amplifier module, which includes two amplifier chains, one for either EGSM900 (in RM-8 and RM-47) or GSM850 (in RM-48) and the other for GSM1800/GSM1900.

Other key components include:

- 26 MHz VCTCXO for frequency reference
- 3296-3980 MHz SHF VCO (super high frequency voltage controlled oscillator)
- front end module comprising a RX/TX switch and two RF bandpass SAW filters
- three additional SAW filters

The control information for the RF is coming from the baseband section of the engine through a serial bus, referred later on as RFBus. This serial bus is used to pass the information about the frequency band, mode of operation, and synthesizer channel for the RF.

In addition, exact timing information and receiver gain settings are transferred through the RFBus. Physically, the bus is located between the baseband ASIC called UPP and Helgo. Using the information obtained from UPP, Helgo controls itself to the required mode of operation and further sends control signals to the front end and power amplifier modules. In addition to the RFBus, there are still other interface signals for the power control loop and VCTCXO control and for the modulated waveforms.

The RF circuitry is located on the top side of the 8 layer PWB.

EMC leakage is prevented by using a metal cans. The RF circuits are separated to two blocks:

- PA, front end module, LNA and 1900 band SAWs
- Helgo RF IC, VCO, VCTCXO, baluns and balanced filters

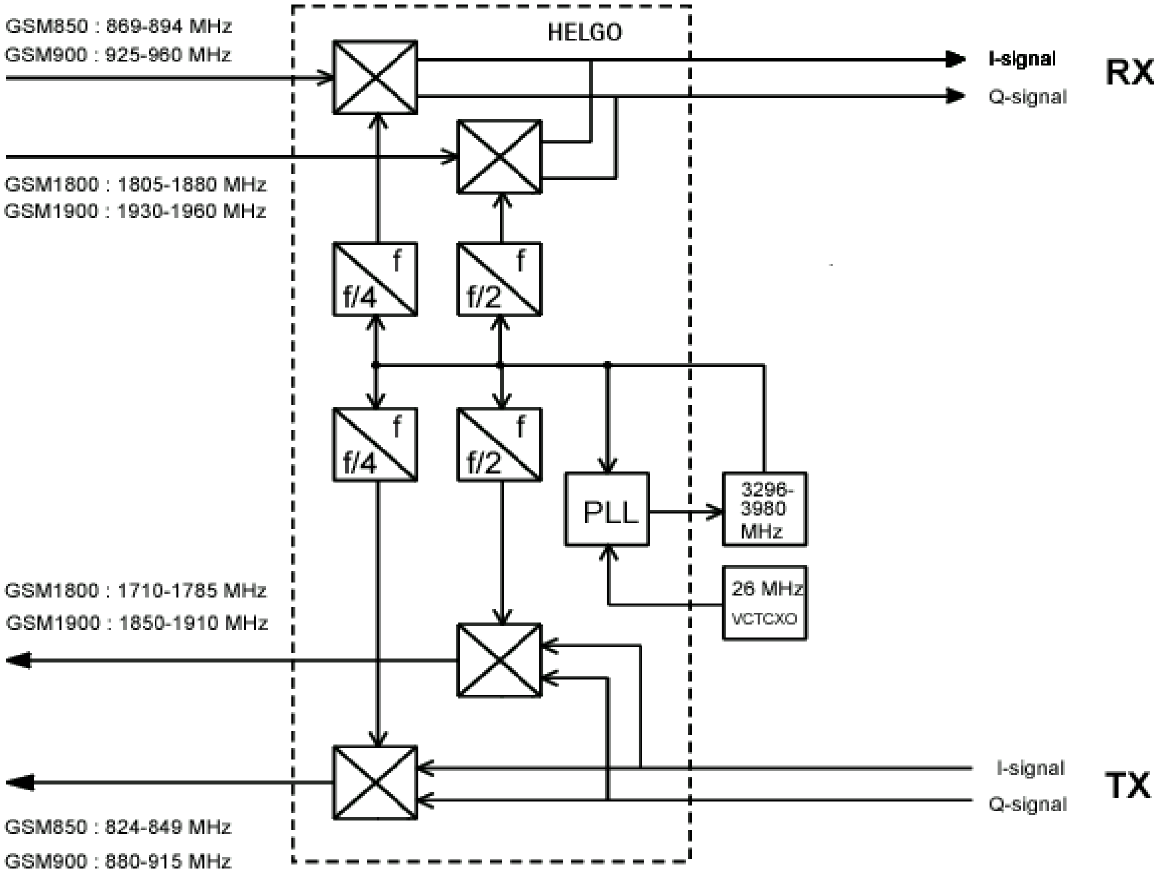
The RF transmission lines constitute of striplines and microstriplines after PA.

The baseband circuitry is located on the one side of the board, which is shielded with a meallized frame and ground plane of the UI-board.

RF Frequency Plan

RF frequency plan is shown below. The VCO operates at the channel frequency multiplied by two or four, depending on the frequency band of operation. This means that the baseband-modulated signals are directly converted up to the transmission frequency and the received RF signals directly down to the baseband frequency.

Figure 18:RF Frequency Plan



DC Characteristics

Regulators

The transceiver baseband section has a multi-function analog ASIC, UEM, which contains among other functions six pieces of 2.78 V linear regulators and a 4.8 V switching regulator.

All regulators can be controlled individually by the 2.78 V logic directly or through a control register.

The use of the regulators can be seen in the power distribution diagram, which is presented in the Figure Power Distribution Diagram below.

The seven regulators are named VR1 to VR7. VrefRF01 and VrefRF02 are used as the reference voltages for the Helgo, VrefRF01 (1.35V) for the bias reference and VrefRF02 (1.35V) for the RX ADC (analog-to-digital converter) reference.

The regulators (except for VR7) are connected to the Helgo. Different modes of operation can be selected inside the Helgo according to the control information coming through the RFBus.

Table 15: List of the needed supply voltages

Table 16:

Volt. Source	Load
VR1	PLL charge pump (4.8 V)

Table 16:

VR2	TX modulators, VPECTRL3s (ALC), driver
VR3	VCTCXO, synthesizer digital parts
VR4	Helgo pre-amps, mixers, DtoS
VR5	dividers, LO-buffers, prescaler
VR6	LNAs, Helgo baseband (Vdd_bb)
VR7	VCO
Vbatt	PA

Typical Current Consumption

The table below shows the typical current consumption in different operation modes.

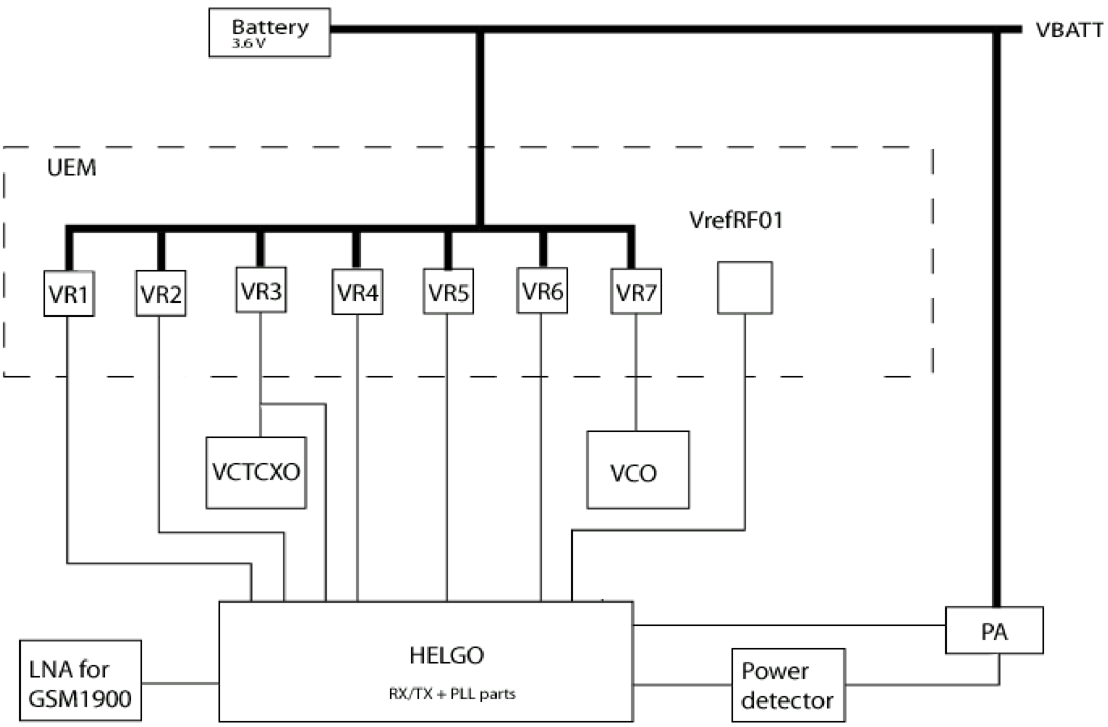
Table 17: Typical current consumption in different operation modes

Table 18:

Operation mode	Current consumption	Notes
Power OFF	< 10 uA	Leakage current (triple band PA)
RX, EGSM900/ GSM850	75 mA, peak	
RX, GSM1800/ GSM1900	70 mA, peak	
TX, power level 5, EGSM900/GSM850	1700 mA, peak	
TX, power level 0, GSM1800/GSM1900	1000 mA, peak	

Power Distribution

Figure 19:Power Distribution Diagram



RF Characteristics

Table 19: Channel Numbers and Frequencies

Table 20:

System	Channel number	TX frequency	RX frequency	Unit
GSM900	0 < =n <=124	F = 890 + 0.2∗n	F = 935 + 0.2∗n	MHz
	975<= n <= 1023	F = 890 + 0.2∗ (n-1024)	F = 935 + 0.2∗(n - 1024)	MHz
GSM850	128 <= n <= 251	F = 824.2 + 0.2∗(n-128)	F = 869.2 + 0.2∗(n-128)	MHz
GSM1800	512 <= n <= 885	F = 1710.2 + 0.2∗ (n-512)	F = 1805.2 + 0.2∗ (n-512)	MHz
GSM1900	512 <= n <=810	F = 1850.2 + 0.2∗ (n-512)	F = 1930.2 + 0.2∗ (n-512)	MHz

Table 21: Main RF Characteristics

Table 22:

Parameter	Unit and value
Cellular system[RM-8/RM-47]] [RM-48]	EGSM900/GSM1800/GSM1900 GSM850/GSM1800/GSM1900
RX Frequency range	GSM850: 869 ... 894 MHz EGSM900: 925 ... 960 MHz GSM1800: 1805...1880 MHz GSM1900: 1930...1990 MHz
TX Frequency range	GSM850: 824 ... 849 MHz EGSM900: 880 ... 915 MHz GSM1800: 1710 ...1785 MHz GSM1900: 1850 …1910 MHz
Duplex spacing	GSM850: 45 Mhz EGSM900: 45 MHz GSM1800: 95 MHz GSM1900: 80 MHz
Channel spacing	200 kHz
Number of RF channels	GSM850: 124 EGSM900: 174 GSM1800: 374 GSM1900: 300
Output Power	GSM850: GSMK 5...33dBm GSM850: 8-PSK 5...27dBm EGSM900: GSMK 5…33 dBm EGSM900: 8-PSK 5…27 dBm GSM1800: GSMK 0…30 dBm GSM1800: 8-PSK 0…26 dBm GSM1900: GSMK 0…30 dBm GSM1900: 8-PSK 0…26 dBm
Number of power levels GMSK	GSM850: 15 EGSM900: 15 GSM1800: 16 GSM1900: 16
Number of power levels 8-PSK	GSM850: 12 EGSM900: 12 GSM1800: 14 GSM1900: 14

Table 23: Transmitter Characteristics

Table 24:

Item	Values (EGSM900/1800/1900)
Type	Direct conversion, nonlinear, FDMA/TDMA
LO frequency range	GSM850: 3296...3395 MHz (4 x TX freq) EGSM900: 3520...3660 MHz (4 x TX freq) GSM1800: 3420...3570 MHz (2 x TX freq) GSM1900: 3700...3820 MHz (2 x TX freq)
Output power (GSM850/EGSM900/GSM1800/GSM1900)	GMSK 33/33/30/30 dBm 8-PSK 27/27/26/26 dBm

Table 25: Receiver Characteristics

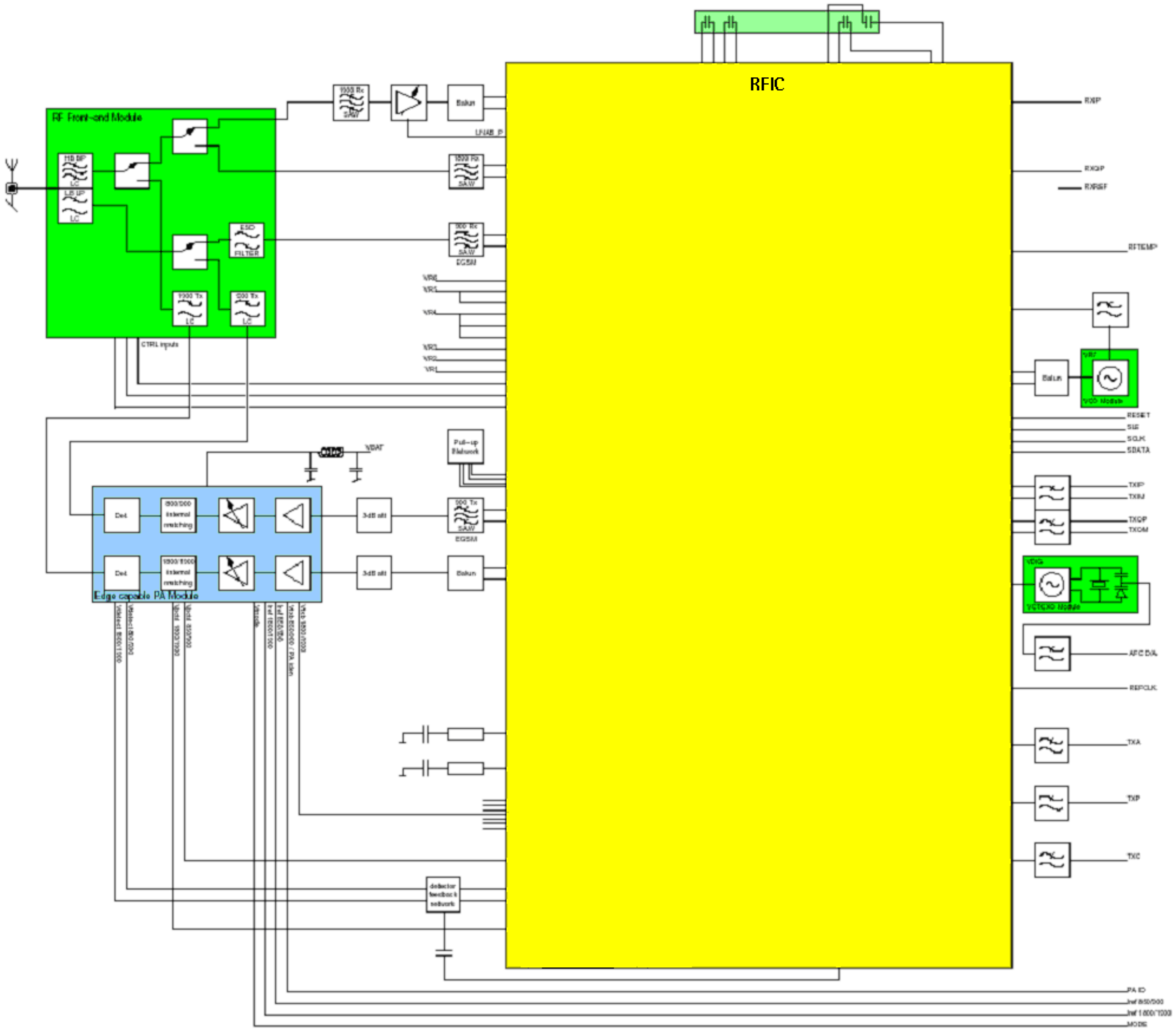
Table 26:

Item	Values, EGSM900/1800/1900
Type	Direct conversion, Linear, FDMA/TDMA
LO frequencies	GSM850: 3476...3575 MHz (4 x RX freq) EGSM900: 3700...3840 MHz (4 x RX freq) GSM1800: 3610...3760 MHz (2 x RX freq) GSM1900: 3860...3980 MHz (2 x RX freq)
Typical 3 dB bandwidth	+/- 91 kHz
Sensitivity	min. - 102 dBm (normal condition)
Total typical receiver voltage gain (from antenna to RX ADC)	86 dB
Receiver output level (RF level -95 dBm)	230 mVpp, single-ended I/Q signals to RX ADCs

RF Block Diagram

The block diagram of the RF module can be seen in the following figure. The detailed functional description is given in the following sections.

Figure 20:RF Block Diagram



Frequency Synthesizers

The VCO frequency is locked by a PLL (phase locked loop) into a stable frequency source given by a VCTCXO, which is running at 26 MHz. The frequency of the VCTCXO is in turn locked into the frequency of the base station with the help of an AFC voltage, which is generated in UEM by an 11 bit D/A converter. The PLL is located in Helgo and it is controlled through the RFBus.

The required frequency dividers for modulator and demodulator mixers are integrated in Helgo.

The loop filter filters out the comparison pulses of the phase detector and generates a DC control voltage to the VCO. The loop filter determines the step response of the PLL (settling time) and contributes to the stability of the loop.

The frequency synthesizer is integrated in Helgo except for the VCTCXO, VCO, and the loop filter.

Receiver

Each receiver path is a direct conversion linear receiver. From the antenna the received RF signal is fed to a front-end module where a diplexer first divides the signal to two separate paths according to the band of operation: either lower, GSM850 or EGSM900 or upper, GSM1800/ GSM1900 path.

Most of the receiver circuitry is included in Helgo.

Transmitter

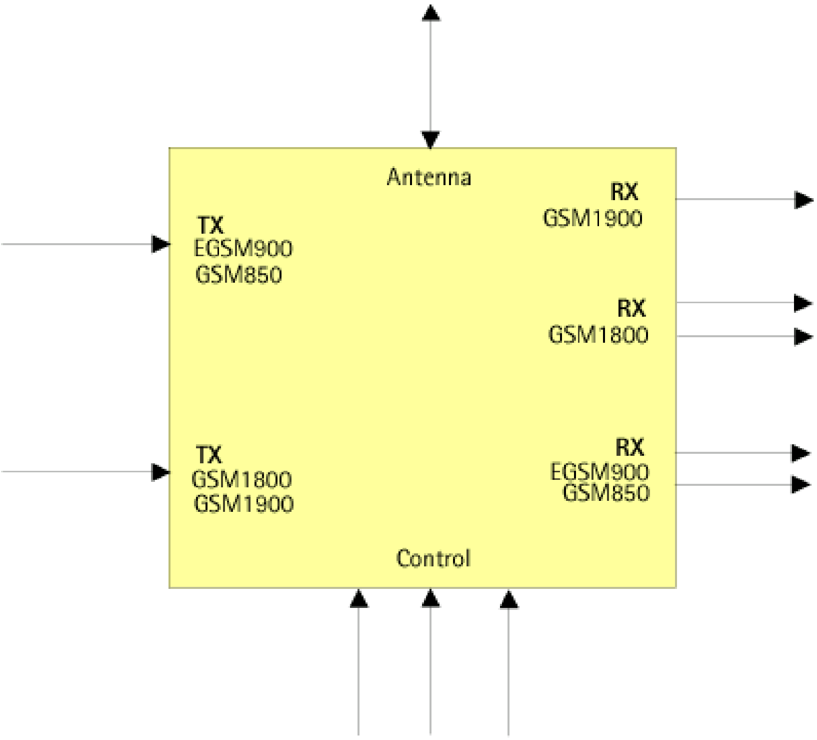
The transmitter consists of two final frequency IQ-modulators and power amplifiers, for the lower and upper bands separately, and a power control loop. The IQ-modulators are integrated in Helgo, as well as the operational amplifiers of the power control loop. The two power amplifiers are located in a single module with power detector. In the GMSK mode the power is controlled by adjusting the DC bias levels of the power amplifiers.

Front End

The front end features include:

- Antenna 50 ohm input
- RX GSM850/EGSM900 balanced output
- RX GSM1800 balanced output
- RX GSM1900 single ended output
- TX GSM850/GSM900 single ended 50 ohm input
- TX GSM1800/GSM1900 single ended 50 ohm input
- 3 control lines from the Helgo

Figure 21:Front End

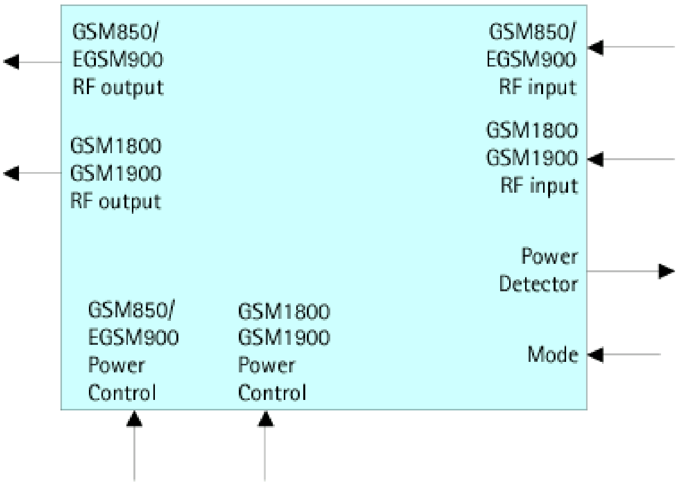


Power Amplifier

The power amplifier features include:

- 50 ohm input and output, GSM850/EGSM900 and GSM1800/GSM1900
- Internal power detector
- GMSK and EDGE mode

Figure 22:Power Amplifier



RF ASIC Helgo

The RF ASIC features include

- Package uBGA108
- Balanced I/Q demodulator and balanced I/Q modulator
- Power control operational amplifier, acts as an error amplifier
- The signal from VCO is balanced, frequencies 3296 to 3980 MHz
- Low noise amplifiers (LNAs) for GSM850/EGSM900 and GSM1800 are integrated

The Helgo can be tested by test points only.

AFC function

AFC is used to lock the transceiver’s clock to the frequency of the base station.

Antenna

The antenna for RM-8/RM-47/RM-48 is a triple band antenna.

Three versions:

- RM-8 EGSM900/GSM1800/GSM1900
- RM-47 EGSM900/GSM1800/GSM1900
- RM-48 GSM850/GSM1800/GSM1900

Antenna concept: Flex foils sticked on the bottom of the upper block B-cover.

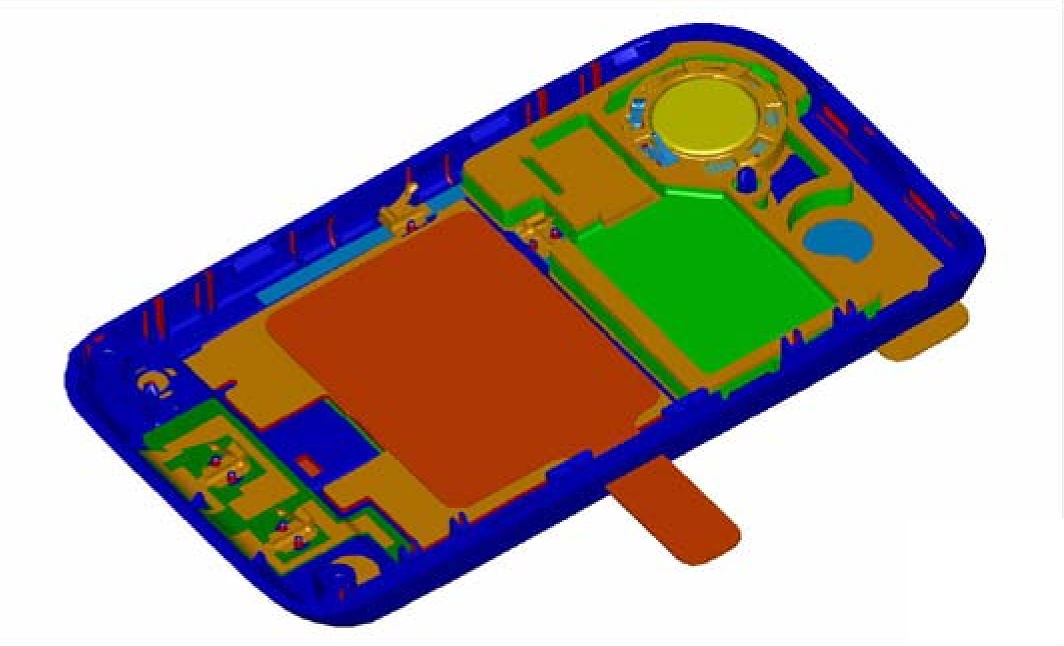


Figure 23:Antenna